

Effects of Augmented Turn-Off™ on Silicon Carbide Module Performance

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Abstract

Switching an SiC MOSFET Power Module creates two significant problems that need to be addressed to optimize the performance of the device: turn-off spikes and ringing. These two parasitic problems need to be controlled while maintaining efficient switching. AgileSwitch has developed a patent-pending line of programmable Gate Drive Boards (GDBs) that address these problems, controlling the turn-off di/dt by varying the gate voltage level and dwell time to one or more intermediate levels during turn-off. This process is typically referred to as Augmented Turn-Off or ATOff.

In addition, AgileSwitch software configurable GDBs report out 7 unique fault conditions along with Temperature and DC Link Voltage. The combination of these effects will help drive growth in adoption of SiC devices, and the inverters that they support.

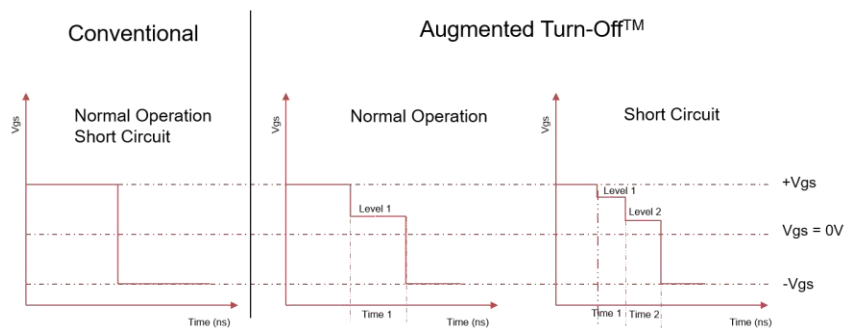


Figure 1 Conventional vs Augmented Turn-Off

Test Configuration

For the purpose of this analysis AgileSwitch selected the ROHM BSM300D12P2E001 MOSFET Module that is rated at 1200V/300A and packaged in the industry standard EconoDual™ footprint. Tests were run at 800V and 266A as a baseline for performance comparisons. Figure 1 shows the circuit used for the analysis. Note the Vds measurement points are the internal Drain and Source terminals on the module. This ensures that any internal stray inductance is part of the analysis.

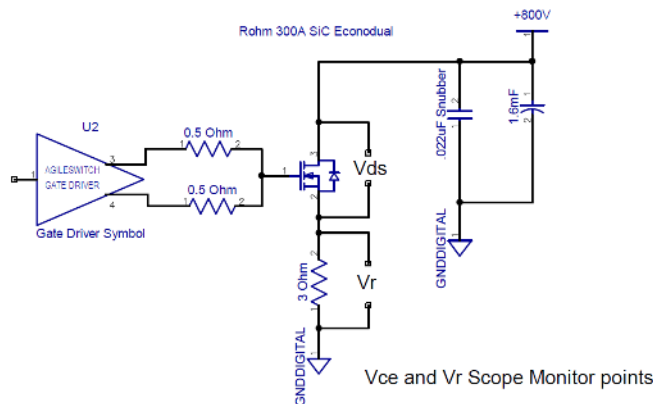


Figure 2: Test Schematic

Baseline – Gate Resistor Control Only

To establish a baseline, AgileSwitch used a GDB without ATOff and changed gate resistor values to demonstrate the effects of resistor change on the turn-off spike, ringing and efficiency. Figure 3 below shows the amount of overshoot and ringing that occurs by using a 1 Ω gate resistor. Blue = V_{ds} , Green = V_{Res} , Purple = $+V_{Gate}$. Note this test could not be run at 800V since the turn off spike exceeded 1200V, so the test was run at 700V.

Figures 4 and 5 show the same operation (now at 800V) but with 5.6 Ω and 10 Ω gate resistors. With a 5.6 Ω gate resistor the overshoot voltage reached 300V, and with the 10 Ω resistor the overshoot voltage is 200V. Note that the switching efficiency is clearly affected. With a 1 Ω gate resistor the switch time is less than 100ns. With a 5.6 Ω gate resistor, the switching time increases to 180ns and with a 10 Ω gate resistor it is almost 300ns.

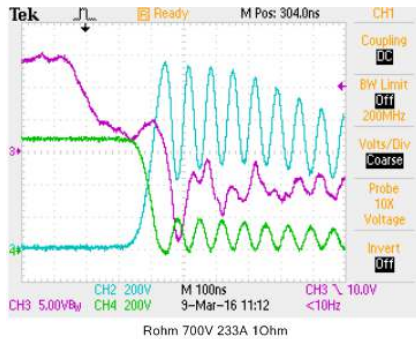


Figure 3: Baseline with 1 Ω Gate Resistors

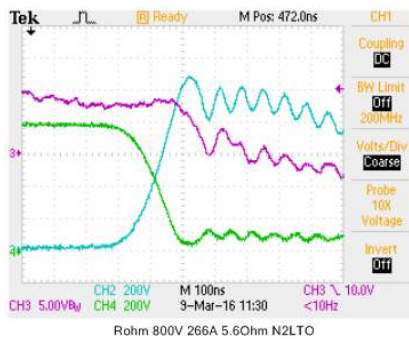


Figure 4: Baseline with 5.6 Ω Gate Resistors

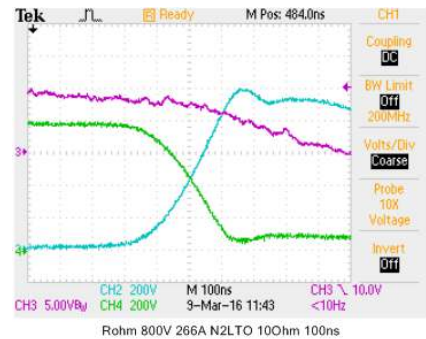


Figure 5: Baseline with 10 Ω Gate Resistors

Augmented Turn-Off Control

The gate voltage level and dwell time utilized in Augmented Turn-Off controls the turn off characteristics of the SiC MOSFET. The next series of scope images show how these two parameters can be modified to optimize the turn-off characteristics of the device

1. Effects of Modifying ATOff Voltage Level

Figures 6, 7 and 8 show how changing the ATOff Voltage level from 4.25V through 4.75V affects the V_{ds} overshoot and ringing when holding the dwell time to 500ns. Gate resistor values of only 0.5 Ω were used in this experiment.

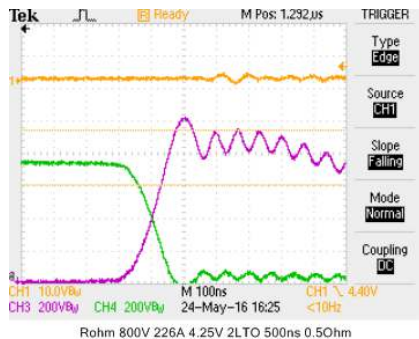


Figure 6: Voltage level = 4.25V

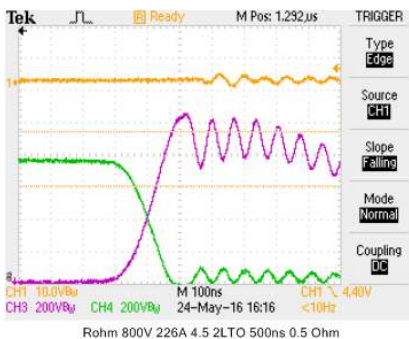


Figure 7: Voltage Level = 4.5V

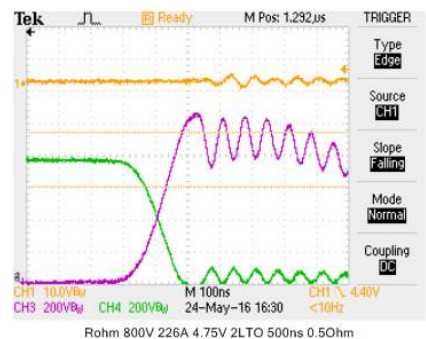


Figure 8: Voltage level = 4.75V

2. Effects of Modifying ATOff Dwell Time

Figures 9, 10, 11 and 12 show the effect of holding the voltage at 4.5 V and adjusting the time from 469ns through 625ns.

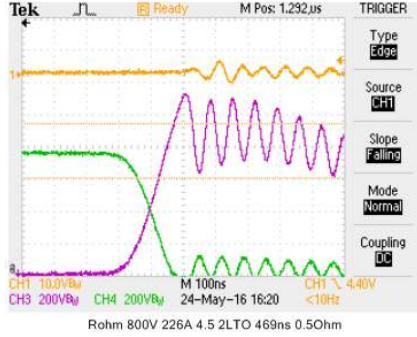


Figure 9: Time = 469ns

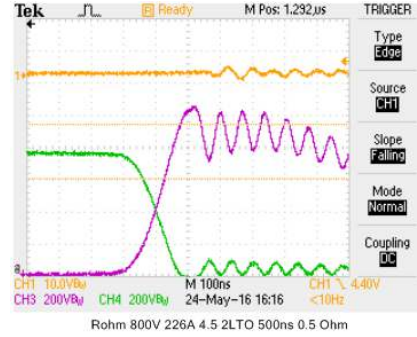


Figure 10: Time = 500ns

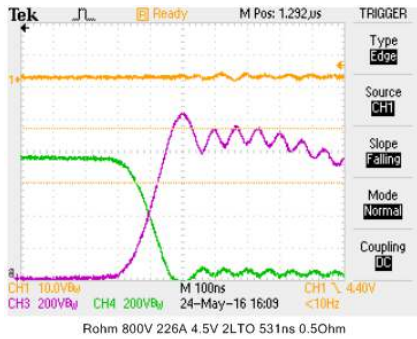


Figure 11: Time = 531ns

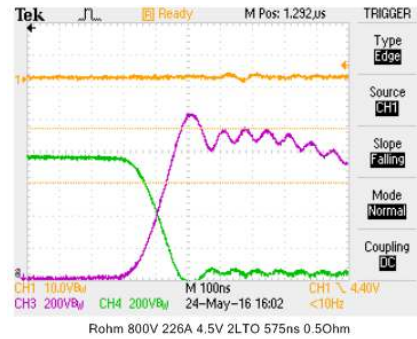


Figure 12: Time = 575ns

3. Effects of Optimizing ATOff Voltage Level and Dwell Time

Figure 13 and 14 shows the impact of holding the voltage at 4.75V while testing two different dwell times: 575ns and 625ns. The results show voltage spikes reduced to only 210 to 220 V, and ringing is reduced dramatically. These results are achieved with gate resistor values of only 0.5 Ω !

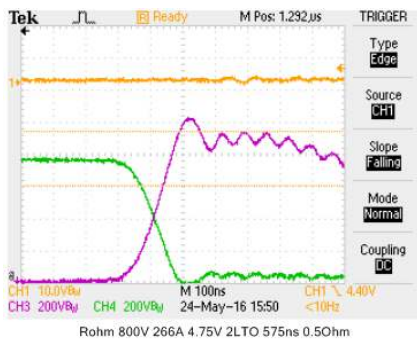


Figure 13: Time = 575ns, Voltage = 4.75V

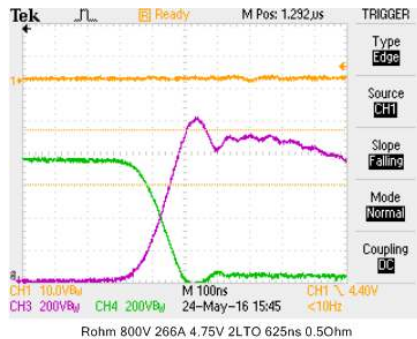


Figure 14: Time = 625ns, Voltage = 4.75V

Effect of ATOff on Efficiency

Comparative efficiency, for purposes of this study, is based on measured E_{OFF} (in mJ) for each scenario. For the examples using gate resistor control only, the following results are obtained:

Gate Resistor (Ω)	E_{OFF} Measured (mJ)	Overshoot (V)
1.0	3.9	450
5.6	8.5	280
10.0	12.5	200

Table 1: Gate Resistor effect on E_{OFF} and Overshoot Voltage

As shown in Table 1, taming voltage overshoot comes at a very high efficiency cost while using gate resistors as a means of controlling this condition.

The following table demonstrates the effects of controlling ATOff voltage level and dwell time to achieve similar results. For example, using 0.5 Ω resistors, overshoot was limited to 220 V, and E_{OFF} of 5.7 mJ was achieved, which is 50% lesser than using a 10 Ω gate resistor only control. This energy savings has significant financial impact, as well as lifetime improvement for the device by reducing the $\Delta T_{ambient-max.}$.

Turn Off Level (V)	Turn Off Time (ns)	E_{OFF} Measured (mJ)	Overshoot (V)
4.25	500	5.7	220
4.50	500	6.0	260
4.75	500	6.2	270
4.50	469	5.3	320
4.50	500	6.0	260
4.50	531	6.2	260
4.50	575	6.4	230
4.75	575	6.4	220
4.75	625	7.1	210

Table 2: 2-Level Turn-off voltage and time sensitivity analysis

Conclusion - Improved Efficiency and Reliability

Through the use of advanced fault detection, monitoring, Augmented Turn-Off, and optimizing the ATOff voltage level and dwell time, AgileSwitch GDBs offer the ideal combination of efficiency and control for SiC MOSFETs. For systems operating at 50kW and up, these benefits translate into significant energy savings and improved lifetime and reliability of the power modules.

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Patents Pending

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