Fast and reliable switching of parallel SiC MOSFET chips in a Half-bridge module

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Abstract

In this paper, the RoadPak SiC power MOSFET half bridge module with multiple parallel chips is presented, which has been designed for stable operation under high speed switching conditions. The module utilizes up to ten MOSFET switches in parallel, reaching an effective current rating of 1100A for 750V rating and 980A for 1.2kV rating. Two module variants are presented; one with gate resistors internal of the module in series with the gate of every chip and one without internal gate resistors. The switching waveforms of both variants are presented and the stable operation for both is demonstrated in extreme switching conditions.

1 Introduction

Among the wide bandgap semiconductor technologies, SiC technology has become increasingly popular among power semiconductor manufacturers during the last years and has been considered the technology which will eventually replace silicon in power converter applications [1]. The low on-state losses and higher switching speed of SiC MOSFET switches compared to the current silicon IGBT technology has made them very attractive alternatives [2], especially for applications where low weight and increased efficiency are critical, such as e-mobility power converters.

However, as much attractive the use of high power SiC MOSFETs as a replacement of Si IGBTs might be, their utilization in high power modules is not straightforward and particular care has to be taken when designing an appropriate package for SiC MOSFET chips. Specifically, due to the constraint imposed by the SiC manufacturing process, the size of a MOSFET must be limited; therefore, several single chips must be paralleled in order to achieve the high current rating required by modern converter applications. Upon paralleling a high number of devices, however, the problem of inhomogeneous switching arises in high speed conditions, leading to increased oscillations and parasitic effects, such as the parasitic turn on of a device [3]-[4]. Such undesired effects can lead to higher power loss [5] and overheating which will ultimately lead to derating or limiting of the switching speed of the module, thus canceling the low loss advantages of SiC MOSFETs.

In this paper, the operation of a high current SiC MOSFET module under high speed switching conditions is demonstrated and the design strategy for utilizing ten SiC MOSFET chips in parallel is discussed. Furthermore, the constraining factors on the switching speed of a high current module and the means to avoid them are analyzed. It is demonstrated, that by choosing an appropriate set of parameters to optimize, it is possible to achieve fast and stable switching, devoid of oscillations and parasitic effects, thus achieving minimum losses.

2 Description of the problem

During paralleling, the mismatch and imbalance between the circuit components of each chip branch are causing uneven dynamic current sharing between chips, as described in [3]-[4]. This effect causes the chips with lower impedance to take up more current than others during dynamic conditions. Additionally, feedback from the current and the voltage of the main (Drain – Source) branch to the gate can influence the switching speed among parallel chips, leading to instability, oscillations and parasitic turn on effects.

In order to avoid these parasitic effects, the need for a balanced design of a power module with multiple parallel SiC chips becomes imperative,

such as the internal circuit components of the module allow the uncompromised parallel operation of the paralleled chips. A successful design will be able to operate in extremely fast switching speeds, thus fully utilizing the SiC MOSFET advantage, without unbalanced oscillations or effects which can prove catastrophic, such as parasitic turn on. In this regard, a balanced coupling between parallel chips was shown to be a key factor [6].

In case optimal switching cannot be achieved, fallback strategies can be utilized, in order to mitigate the adverse effects of feedback, such as using additional gate resistors for each parallel chip inside the module. These resistors are filtering the effect of current and voltage feedback to the gate of the chips and prevent them from spreading to the nearby gates. However, such a design option leads to higher cost, lower reliability due to additional process steps to incorporate the internal resistor and ultimately to higher losses.

3 Effect of parasitics on SiC module design

There have been various attempts to quantify the effects of parasitic components on the oscillations of SiC MOSFETs and propose methods for optimizing performance of the SiC chips both on single chip and multiple parallel chip operation [7]-[13]. However, the mathematical analysis of a circuit becomes increasingly complex when the number of chip increases and there does not seem to be a consensus on the circuit parameters which affect the switching quality of paralleled chips. Moreover, effects like the parasitic inductive coupling between different paths of the circuit tend to be ignored in the analysis; these effects, however, are becoming increasingly important when the switching speed of the module increases. For example, a switching speed of 30 A/ns will give a voltage raise (or drop) of 3V over a mere 100pH of mutual coupling inductance, which is already a very high voltage increase when taking into account that the threshold voltage of SiC MOSFETs is close to V_{gsth} = 2V.

Additionally to the circuit parameter mismatch, the mismatch of chip parameters between each other is also a source of uncertainty when designing a SiC power module. A parameter variation of up to ± 20% between chips is not unheard of for all the parameters of the MOSFETs. This variation can lead to unbalanced switching between parallel SiC chips even when the circuit parameters are identical. The effect of the parameter mismatch between chips has been analyzed in [4].

From the above analysis, it can be concluded that designing a module which houses multiple SiC MOSFETs is an extremely sensitive process and focusing on the correct optimization targets can make the difference between balanced and smooth switching and uncontrolled catastrophe. There have been efforts to introduce additional components which will force balanced switching in the literature. For example, methods to suppress oscillations using couple inductors have been proposed in [14] – [15].

Despite the efforts to come up with the optimal method for applying paralleled SiC MOSFET operation, the actual design of a module with multiple paralleled chips remains an unsolved issue and the process of obtaining a robust module layout involves trial and error process and multiple learning cycles.

4 The RoadPak SiC module

In this paper, the RoadPak half bridge module is presented, which has been specifically designed to house up to ten parallel SiC MOSFET chips, reaching a current rating of 1100A at 750V and 980A at 1200V. The module is capable of successfully switching at extremely fast switching speeds, up to 25 and 35 V/ns respective to each voltage class and maintains stable operation even with gate resistor values as low as 0.15 Ohm.

For the design of the module, focus was given on obtaining a balanced layout for the main and gate inductances, within a certain optimization window. Additionally, balancing the coupling inductance between the main (Drain - Source) loop and the auxiliary (Gate – Source) loop of each single chip was chosen as an optimization target. This differs from the analysis of Ch. 3 in the sense that the self-inductance of the gate and source path as well as the mutual inductance between main and auxiliary path is included in the consideration. With the selected optimization target, effects which start to demonstrate at very high switching speeds are also considered and their optimization leads to faster switching capability.

In a high current density module such as the RoadPak, the space within the module substrate is precious; therefore the placement of the chips within on the substrate has to be strategically laid out in order to achieve maximum current rating without compromising on the ability of the thermal stack to dissipate the lost energy. One of the strategic choices which enabled the maximization of the current capability of the module was not to include a separate kelvin source for the gate connection on the chips. This might seem counter

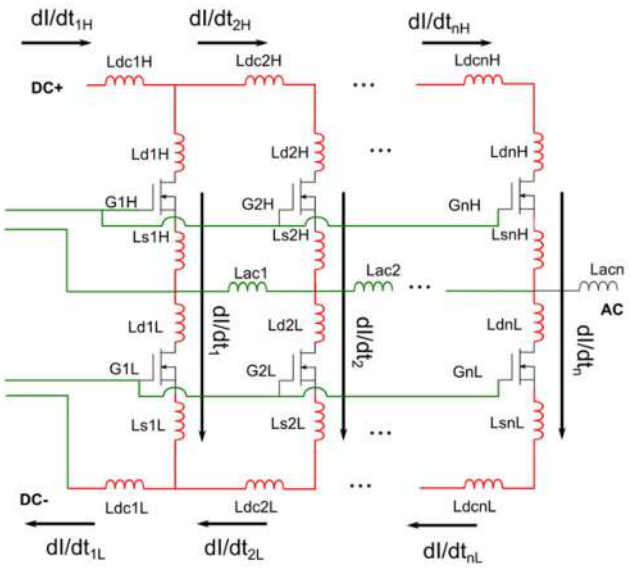

Fig. 1: Illustration of the main loop inductance path (red) and the gate path (green) of the RoadPak module. For reasons of readability, the inductance of the gate paths are omitted in the drawing.

intuitive, but it will be demonstrated that the careful choice of chip and lead placement has achieved a module design with robust, oscillation free performance even at extremely high switching speeds.

The main target of the design was chosen to be the achievement of a small negative value for the gate coupling inductance. The reason for this choice was to include the inductive voltage drop due to the current slope as well as the coupled inductive voltage drop due to indirect current paths. This effect is demonstrated in Fig. 1. In the figure, the inductances involved in the gate path only are omitted for simplicity. The current slopes drawn with an arrow represent the direction of the dI/dt during a MOSFET turn on event of each side, or, equally, the body diode turn off event of the opposite side. Normally, the effect of the source self-inductance only is included in the calculation of the parasitic behavior on the gate path. During the optimization of the RoadPak, additionally to the source self-inductance, the effect of the mutual inductance of all the current paths with the gate path of each chip was considered and optimized. The result of this optimization is demonstrated in Fig. 2. It is shown, that the total gate coupling is optimized within a window of 3 pH for the low side and 5 pH for the high side.

The negative value of the total coupling inductance was chosen in order to achieve a small negative

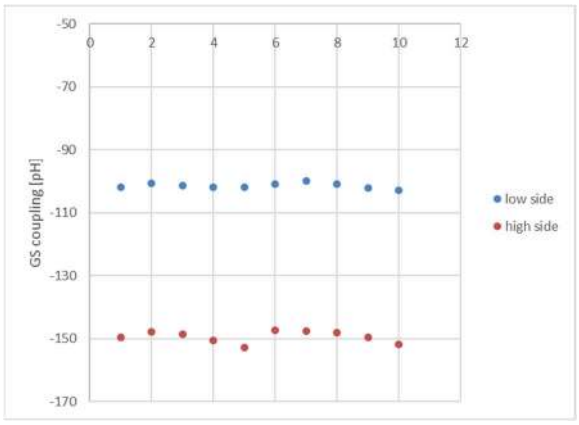

Fig. 2: Gate coupling value per chip position (x axis) for the high side and low side

feedback on the gate. This will cause the increasing current to apply a negative voltage on the gate. In the event of MOSFET turn on, the negative feedback will decrease the gate voltage, effectively slowing down the turn on of each individual chip. A positive feedback would increase the gate voltage, leading to uncontrollable speed up of the turn on and large imbalance. A very high negative value would cause the module to become too slow and the overall losses too high. The same analysis can be done for a MOSFET turn off event. The negative gate coupling prevents the current of each individual chip to turn off too fast, therefore increasing balancing of the current and reducing the oscillations.

In the event that the optimization window would nevertheless prove not enough to suppress gate oscillations, a fallback design was considered. An additional design with gate resistors placed on each chip gate path inside the module was implemented. This design was thought to have a positive impact on the oscillations, because it would provide damping on the gate paths and reduce the crosstalk between the chips. However, the actual use of the internal gate resistors in the module is not desired, because it increases the overall cost of the module. Moreover, the increased number of processes needed to integrate gate resistors into the module might lead to increased process errors and reduced reliability.

In this paper both design variants, with and without per chip gate resistors are demonstrated. It is shown, that the module presents equally stable switching curves either with or without internal gate resistor, owing to the balanced internal design of the modules. The switching waveforms of the module are presented in order to demonstrate the stable and reliable switching in both cases.

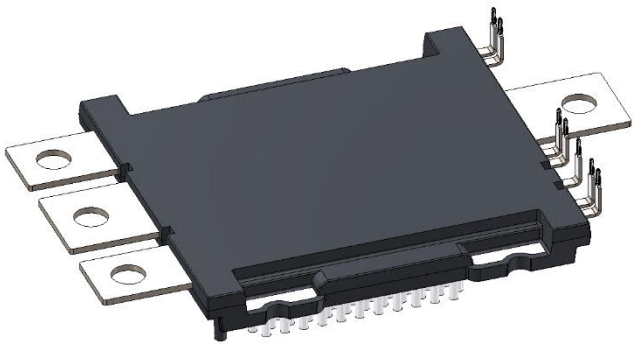

Fig. 3: The RoadPak SiC MOSFET half bridge module

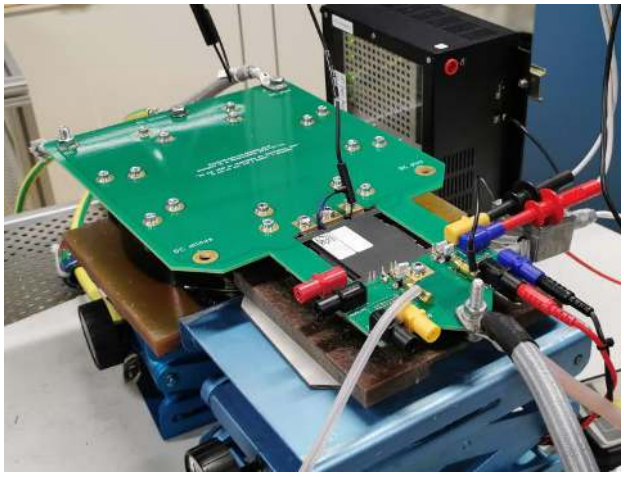

Fig. 4: Test setup for the RoadPak double pulse test. The overall main loop stray inductance is 10nH

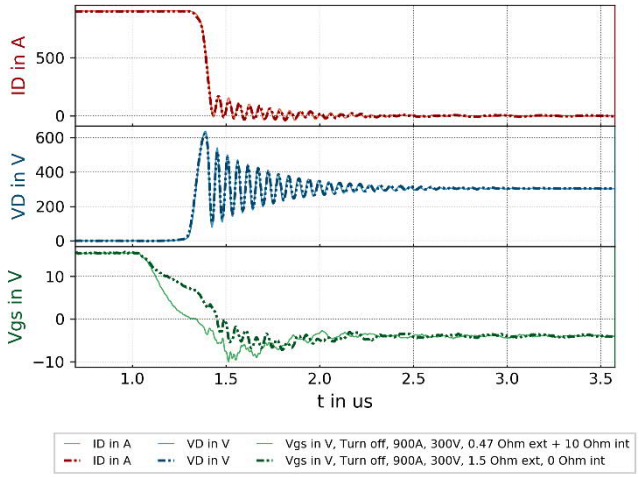

Fig. 5: MOSFET turn off with external gate resistor only (dashed) and with internal plus external gate resistor (continuous).

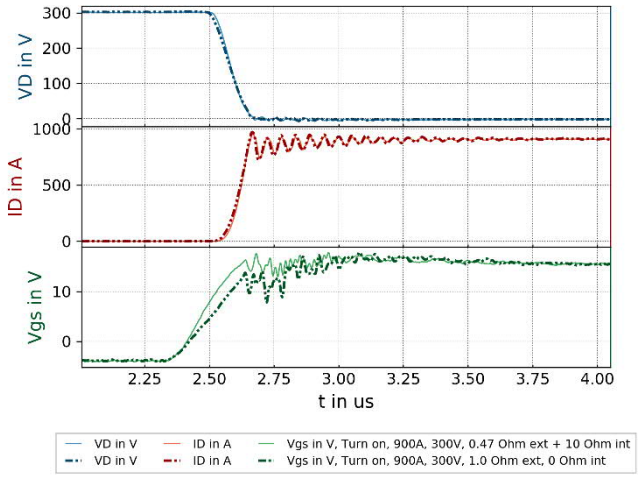

Fig. 6: MOSFET turn on with external gate resistor only (dashed) and with internal plus external gate resistor (continuous).

5 Test results

The implementation of the design strategy, as described in chapter 4 resulted in the RoadPak SiC MOSFET half bridge module which is illustrated in Fig. 3. The module was tested using a double pulse test on a test rig with a ring capacitor and a printed circuit board, in order to achieve low stray inductance for the main commutation loop. The test rig is depicted in Fig. 4 and has an overall commutation inductance of 10 nH.

Due to the unavailability of a dedicated gate driver unit for the RoadPak module, generic laboratory gate drivers were used for the double pulse tests. The drawback of this setup is the high gate inductance, which might cause oscillation during the switching. This oscillation can be observed in the following waveforms, however, compared to the SiC chip induced oscillations, its time constant is much longer and has minimal effect on the measurements. In order to stabilize the gate voltage and compensate for the long cable, additional gate capacitors were placed on the gate of the order of 50 ~ 100 nF. The described setup will give an impression of the switching behavior of the module; however it is not ideal and a dedicated gate driver unit is recommended for proper testing.

In Fig. 5 and 6, the respective MOSFET turn off, and MOSFET turn on of a 750V, 10 chip module is demonstrated. The waveform of a module without per chip internal module resistors is compared against the waveform of a module with 10 Ohm internal resistor. Because of the paralleling of the chips, the 10 Ohm internal resistance per chip is equivalent to 1 Ohm of total gate resistance on module level. This equivalence is apparent during

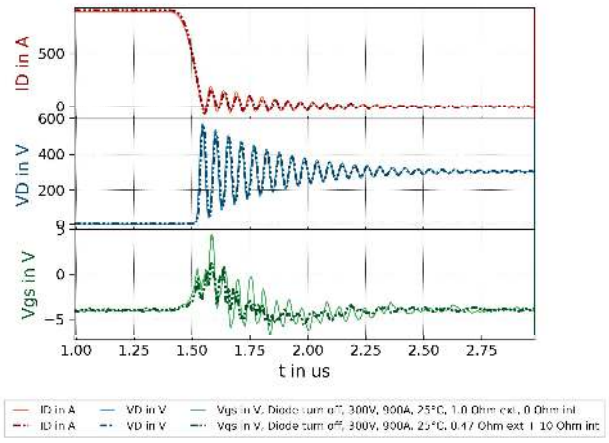

Fig. 7: Diode turn off with external gate resistor only (continuous) and with internal plus external gate resistor (dashed).

the turn off of Fig. 5, because the drain current and drain voltage waveforms are identical for the two cases where the total equivalent gate resistance for both module build-ups (external only and combined internal and resistor) equals to 1.5 Ohm. The waveform of the turn on (Fig. 6) has similar characteristics, however, the module without internal resistors tends to be marginally slower.

The switching of the body diode is depicted in Fig. 7. The two module versions are again compared against each other, where they present identical stable behavior. It can be observed that the module with the internal resistors has lower oscillations at the gate, but this is the effect of the voltage division between internal and external resistors and is not representative of the actual voltage which is applied on the chip gate. In any case, no parasitic turn on is observed, which means that the voltage at the gate of every chip is stable and below the threshold.

The excellent tunability of the switching of the module is also presented in Fig. 8. The optimized design, as presented in Ch. 4 enables controlling the dV/dt (switching speed) by adjusting the external resistance of the module at the gate driver. It is observed that the module is equally tunable with internal or external resistor. However, the version with the internal resistor might not reach high speed as required. In any case, the module is well balanced and tunable, which gives flexibility to match customer requirement. In Fig. 9, the effect of increasing the gate resistance at the gate driver is observed. The switching oscillations of the drain voltage, which are inherent for a SiC module, can be reduced by reducing the switching

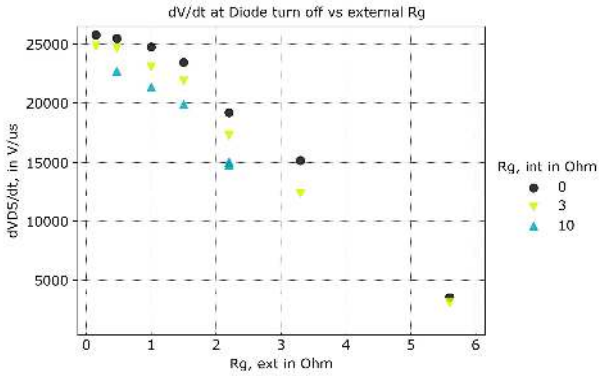

Fig. 8: Switching speed versus external gate resistance at Diode turn off, for 3 different module build ups: 0, 3 and 10 Ohms of internal gate resistance.

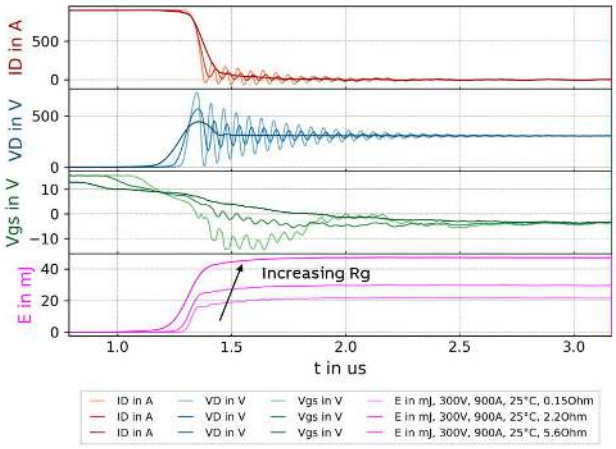

Fig. 9: Tuning the switching speed with an external Rg. The drain oscillations can be reduced at the cost of higher losses.

speed; however, this will cause the losses to increase.

The turn off and turn on of the 1.2kV module is illustrated in Fig. 10 and Fig. 11 respectively. In this case the behavior of the chip is inherently differently due to the chip design difference. The oscillations of the drain voltage are less intense compared with the 750V module. Additionally, the gate oscillations seem to be more intense in the 1.2kV module. This is partly due to the fact that the voltage slope is much higher when the voltage becomes higher and therefore the capacitive coupling due to the miller capacitance is much stronger. Nevertheless, both the turn off and the turn on of the module is robust and the oscillations of the current and drain voltage are limited.

For the turn on, it is observed that the current presents higher overshoot compared to the 750V

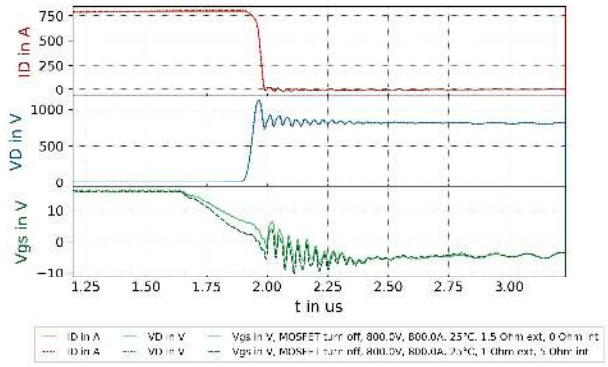

Fig.10: MOSFET turn off with external gate resistor only (continuous) and with internal plus external gate resistor (dashed).

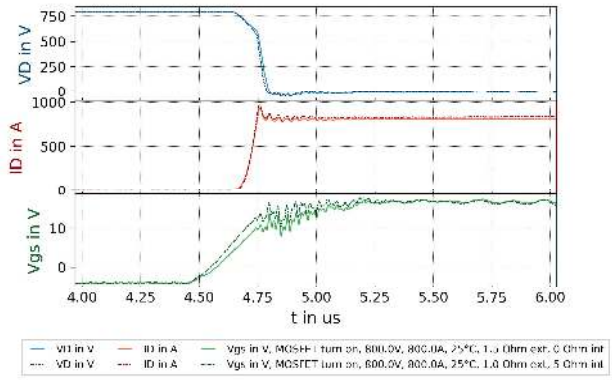

Fig. 11:MOSFET turn on with external gate resistor only (continuous) and with internal plus external gate resistor (dashed).

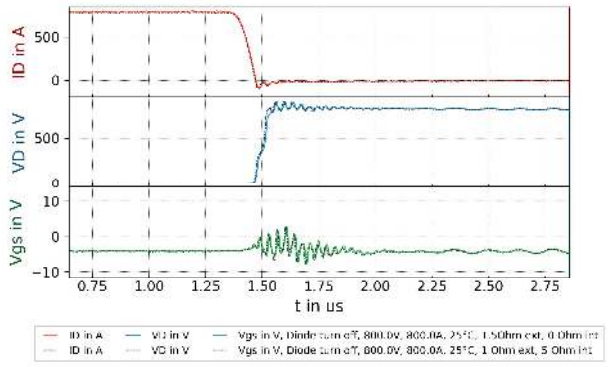

Fig. 12: Diode turn off with external gate resistor only (continuous) and with internal plus external gate resistor (dashed).

version. This is due to the design of the chip body diode, which has a higher recovery current compared to the 750V chip body diode.

The body diode turn off of the module is illustrated in Fig. 12. It is observed that the drain voltage is

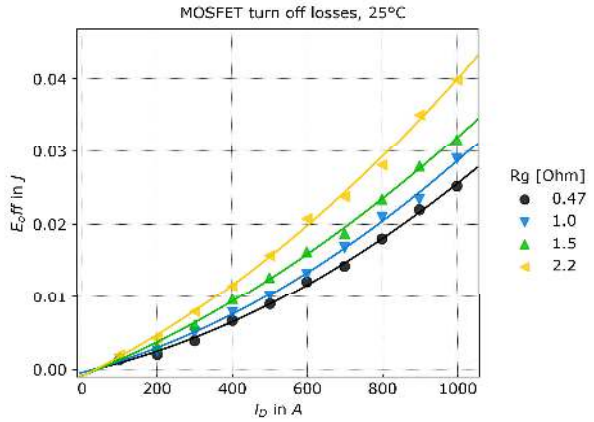

Fig. 13: Turn off losses of the 1.2kV, 20 chip module with a DC link voltage of 800V and stray inductance of 10nH. The module has no internal gate resistor.

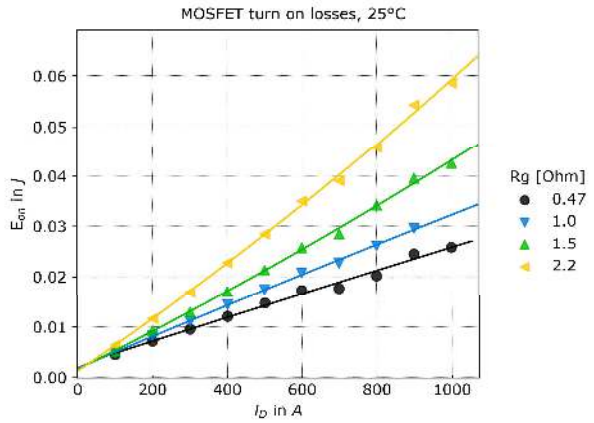

Fig. 14: Turn on losses of the 1.2kV, 20 chip module with a DC link voltage of 800V and stray inductance of 10nH. The module has no internal gate resistor.

much smoother without a lot of oscillations compared to the 750V module. Reason for that is the increased reverse recovery current of the 1.2kV chip which makes transition smoother.

The comparison between the external and the internal resistance version of the module shows that the module is stable both with and without internal resistance and the contribution of the internal gate resistance on the reduction of the oscillations is marginal, which is the effect of the optimized electromagnetic design of the module.

On Fig. 13 and Fig. 14 the measured turn off and turn on losses are presented, respectively. The measurements were made with a DC link voltage of 800V and a stray inductance of 10nH. The

module which was used for these measurements had no internal gate resistor, so the total equivalent switching resistance is the one noted in the graph. The diode turn off losses are not illustrated, because they are an order of magnitude lower and therefore their contribution to the overall losses is negligible.

Regarding the switching speed, the 1.2kV module reaches up to 35 V/ns during switching with the lowest resistance (0.47 Ohm). This switching condition, however, is too fast to be useable at the application, because at the highest currents (> 800A) the voltage of the drain surpasses the maximum of 1.2kV. A much more useable condition is the case of turning off with 1.5 Ohm gate resistor, which reaches up to 25 ~ 30 V/ ns. The effect of the stray inductance of the commutation loop should also be considered, because it has major contribution to the switching losses. An increase from 10nH to 20nH will increase the turn off losses for the same switching speed and additionally lowering the switching speed is required due to overvoltage. Therefore, the need for careful design of the busbar and the commutation loop is imperative for the effective use of SiC MOSFET modules.

6 Conclusion

In this paper, the RoadPak SiC MOSFET half bridge module is presented and the electro-magnetic optimization strategy for its design is analyzed. It is shown that, by choosing the optimization target as the balancing of the coupling inductance of the chip gate – source path, reliable operation of multiple parallel SiC MOSFET chips is achieved. A fallback strategy for the mitigation of the propagation of gate oscillations by utilizing gate resistors per each chip gate, internal of the module, is discussed. The results of two different chips with 750V and 1.2kV rated voltage respectively and 10 chips in parallel are presented. It is demonstrated that the switching is robust without additional unstable oscillations due to the chip paralleling. It is further shown that the internal gate resistor has minor effect on reducing oscillations during switching and the electro-magnetic design of the module is enough to prevent imbalances and strong parasitic effects.

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