High performance DC link capacitor/bus sourcing dual Infineon HybridPACK™ Drive inverters for EV applications

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The Power Point Presentation will be available after the conference.

Abstract

A high performance integrated capacitor / bus for the Infineon HybridPACK™ Drive was presented previously [1]. This foundation will now be used as the basis for evaluating a single DC link capacitor / bus to support two HybridPACK™ Drive inverter stages, thus enabling a significant improvement in power density, weight and cost for high performance EV applications. Detailed knowledge of the drive cycle is required along with full thermal characterization to demonstrate the required life. Transient thermal simulation results and experimental data are provided. These results are utilized to define practical topologies and power limits for one DC link feeding two HybridPACK™ Drive modules for dual motor in-board drive applications.

1.0 Introduction

A low-inductance DC link enables IGBT operation at the highest possible switching speed and maximum working voltage for optimal efficiency. The SBE 700A186 cap/bus test kit has been previously demonstrated to enable such efficient operation for the Infineon HybridPACK™ Drive module while also supporting inverter operation up to 150kW peak power [1]. Many customers are now utilizing dual IGBT modules for next generation EV designs. This begs the question of whether a single cap/bus assembly can source the ripple current required by two parallel inverter stages to reduce volume, weight and cost while still achieving low ESL as shown in Figure 1.

Fig. 1. Illustration of a single integrated cap / bus (SBE 700A243) sourcing two Infineon HybridPACK™ drive IGBT modules.

This is very relevant for high performance dual motor in-board drive electric vehicle platforms where a significant cost and weight reduction is possible using only one DC link. Such an approach requires careful optimization at the system level and consideration of multiple parameters including

1) Drive cycle – voltage, current, and coolant temperature
2) Modulation control scheme
3) Thermal time constants
4) Heat loading to the capacitor from the IGBT and bus
5) Thermal boundary conditions

A detailed simulation approach is utilized to evaluate the single cap/bus sourcing parallel inverter stages. The two-dimensional results presented previously are used as the basis for validating a complete three-dimensional model. A full three-dimensional analysis is then undertaken to consider the effect of bus heating and connection topology. Temperature rise testing of an instrumented capacitor/bus assembly subject to defined thermal boundary conditions and ripple current provides an empirical validation of the model. From this point, the model is utilized to consider a very high performance use case and compute the capacitor hotspot temperature subject to continuous and peak operating transients and heating of the bus conductors.

2.0 Simulation

The complete 700A243 capacitor/bus geometry is imported via step file into the Flux3D™[2] finite element analysis package. In order to reduce the size of the mesh, non-essential mechanical features such as fasteners are eliminated. Note that the mesh effectively defines an equivalent thermal circuit for the problem in matrix form. The bus bar insulation is treated using a thin region model with a defined thickness and thermal conductivity such that meshing of these regions is not needed. Even with these simplifications, the domain size is significant with 177,285 nodes and 945,962 first order volumetric elements. The external mesh is illustrated in Figure 2 which also defines the boundary conditions. Note that the capacitor/bus must be cooled from the bus side (potentially sharing cooling infrastructure with the IGBT modules) to achieve the best performance. For a worst case analysis all other surfaces are treated as adiabatic (perfect thermal insulation with no heat flow).

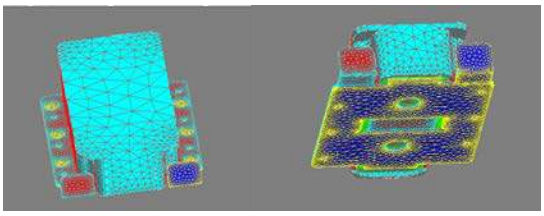

Fig. 2. Finite element domain and boundary conditions for 3D simulation

A DC conduction finite element model (FEM) was utilized to compute the ESR of the capacitor terminals and bus bars for the following scenarios:

1) IGBT connections through capacitor (sourcing ripple current): 30.0μΩ
2) DC tabs through IGBT connections (DC component): 39.4μΩ

These numbers are scaled to the appropriate frequency (skin depth) and temperature to allow computation of the bus and terminal losses for the capacitor ripple current and DC bus current. The capacitor winding ESR is calculated using a proprietary analysis package which incorporates empirical temperature coefficients for DC leakage, dielectric dissipation, and electrode losses. The nominal ESR for the capacitor assembly comprised of two 250μF windings in parallel is 300μΩ assuming 500Vdc operation at 20kHz. Note that the winding electrode losses are spatially dependent and superimposed on the uniform dielectric dissipation and DC leakage losses in the 3D finite element model. The capacitor temperature rise is driven by the internal losses and effective thermal resistance to the cooling plate superimposed on the bus losses (DC and ripple) and corresponding thermal resistances to the cold plate. The bus losses can be a significant contributor to capacitor temperature rise, particularly at peak DC current.

Having defined the thermal sources, the geometry is evaluated using a static thermal analysis which accounts for the temperature dependence and any anisotropy of the thermal conductivities in each material. The output is the steady state thermal solution at full equilibrium from which mean temperatures can be computed to validate that correct material properties have been utilized for loss calculations. Additional iterations can be performed if needed to be certain that there is no issue with thermal runaway in the system. Finally, temperature dependent specific heat data is added and a full transient thermal simulation is performed to look at the time constants, which must be understood relative to the drive cycle. Note that the simulation is calibrated against testing described in the following section to validate all of the assumptions.

3.0 Ripple Current Testing

Calibration of finite element analysis against actual capacitor temperature rise measurements subject to ripple current and defined boundary conditions has been reported previously using a 2D model [3]. SBE used its 20kHz resonant power supply that can source up to 500Arms to a DC link capacitor/bus structure. The high current connections are temperature controlled to minimize heat flow to or from the test object. Water cooled plates can be placed on one or both sides of the device being tested to set boundary conditions. The SBE 700A243 DC link cap/bus is shown connected to the test fixture in Figure 3. Note that a gap pad is used between the bus and the cooling plate. A mirror image arrangement is applied to the case (top) side and fiberglass insulation is placed around the sides to minimize heat leakage. For the calibration of the model, the use of bus and case side cooling is the easiest scenario since stray heat flow is minimized.

Fig. 3. SBE 700A243 500μF 500V integrated capacitor/bus installed on cooling plate and connected to ripple current source for temperature rise testing.

hofer eds (**e**lectric **d**rive **s**ystems) was asked to specify parameters for two inverter stages running in parallel. The parameters were set as a continuous AC phase current of 320Arms (160Arms for each HybridPACK™ Drive). In order to make a very aggressive test, the capacitor/bus was run at 320Arms current to equilibrium with both cooling plates set at 65°C (a typical cooling fluid temperature) and the empirical results are presented in the solid blue, red, and green curves of Figure 4. Note that three thermocouples are installed on each winding with one inside the core close to the hotspot and one on each end spray face. Note further that the actual capacitor ripple current would be only around 2/3 of this value. The results between the two windings are almost perfectly matched, so just one set of thermocouple readings is shown. The blue, red, and green curves with square markers in Figure 4 show the simulation results which are much more pessimistic since only case and bus cooling are considered. In reality, the experiment will have some heat lost to the input connections which are air cooled to 65°C to avoid adding additional heat load. Accounting for cooling via the IGBT connections, a reasonable fit is achieved as shown with the blue, red, and green curves with dashed lined and circle markers in Figure 4. Note that the core thermocouples show a slower, more "concave" ramp since they are more isolated while the end spray thermocouples show a faster more "convex" ramp due to tight thermal coupling to the bus. The results agree to within better than 5°C and the simulation is still a bit more conservative since the insulation around the case is not perfect in the actual test.

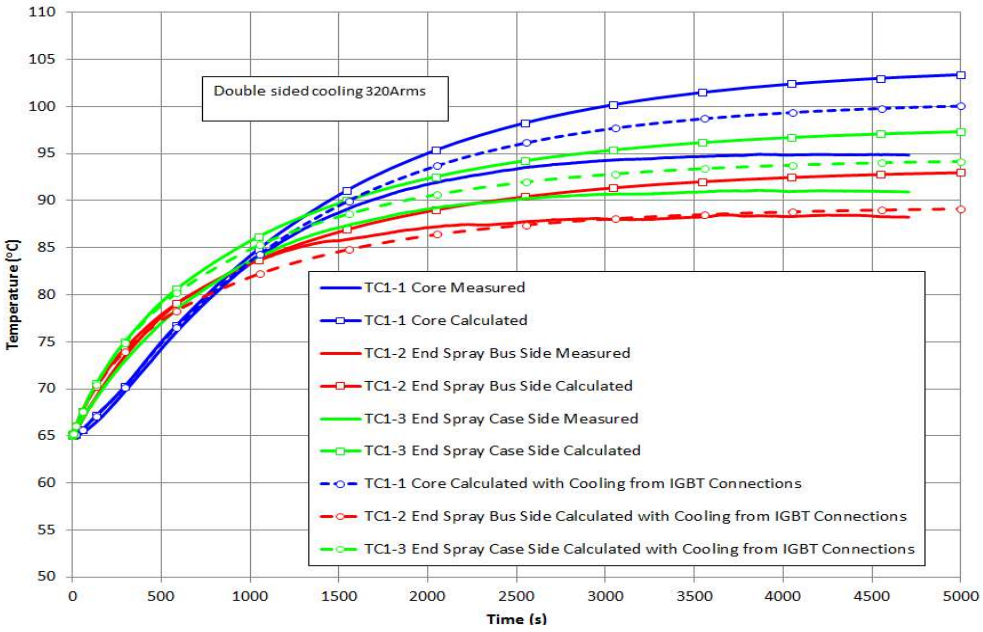

Fig. 4. Calibration of the capacitor/bus transient thermal finite element analysis against measured data at 320Arms and 20kHz with 65°C cooling applied to the case and bus.

4.0 Drive Cycle

The drive cycle must be understood in conjunction with the thermal model to assess how much time is spent at various voltage and temperature stress conditions. From this, the total amount of life consumed at each condition can be calculated and the overall life defined.

The first step is to look at feasibility of driving two inverter stages from the single DC link subject to continuous and peak operation.

Engineers from the hofer eds team have defined the following parameters for evaluation:

1) Continuous operation
   a. DC current 250A
   b. IGBT module phase current 160Arms
   c. EM phase current (current sum inside 6 phase EM) 320Arms
   d. Capacitor ripple current 192Arms
2) Peak operation (30 seconds)
   a. DC current 1000A
   b. IGBT module phase current 480Arms
   c. EM phase current (current sum inside 6 phase EM) 960Arms
   d. Capacitor ripple current 580Arms
3) With interleaved PWM, capacitor ripple current can be reduced nearly up to 50%

A frequency of 20kHz is assumed for the ripple current along with access to a cooling plate at 65°C. Note that both DC and ripple current heating in the bus are considered and that the bus is tied to the cooling plate through an optimal gap pad. In effect, the capacitor hotspot temperature will rise to some level above the bus temperature.

A significant reduction of the total capacitor ripple current can be realized with PWM Interleave. According to theoretical considerations the minimum achievable capacitor ripple current is related with a PWM phase shift of 90° between the two three-phase power stages (HybridPACK™ Drive). This assumption was proven by simulation using space-vector modulation with the results shown in Figure 5.

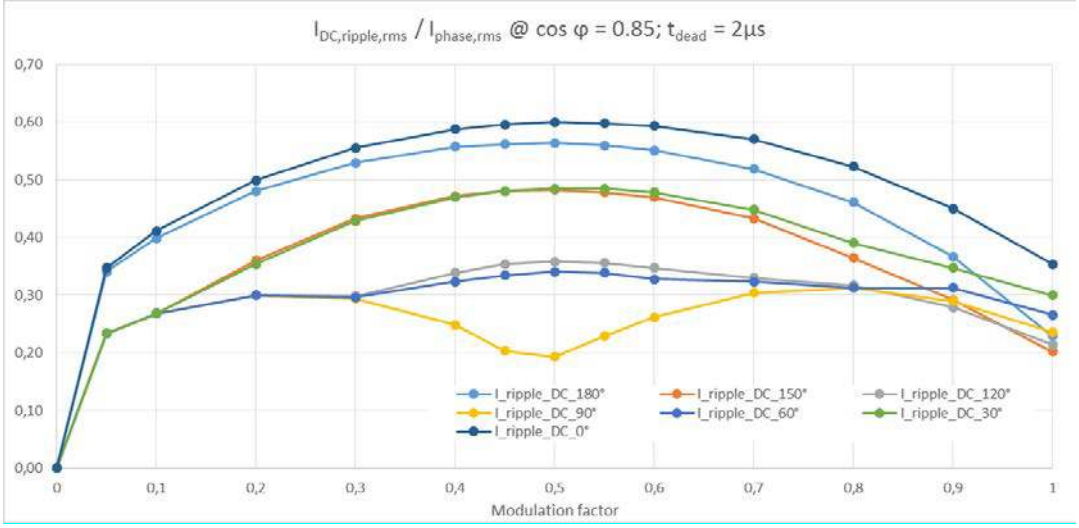

Fig. 5. Capacitor ripple current normalized to phase current over modulation factor for different PWM phase-shift values

5.0 Capacitor/Bus Rating

The 700A243 was first evaluated to the drive conditions defined in the previous section using the calibrated finite element model with the following assumptions:

1) Heat is only extracted from the external surface of the bus, all other surfaces are adiabatic
2) A high performance gap pad is utilized such that the bus bar insulation is the limiting thermal resistance
3) No heating or cooling from IGBT terminals
4) No heating or cooling from DC inputs
5) Account for ripple current losses in capacitor and terminals
6) Account for ripple current and DC current losses in the bus and DC tabs

Losses are computed for the capacitor winding, capacitor terminals, and bus conductors including DC tabs using the approach defined in the simulation section. Additional discussion of heating from the IGBT terminals will be considered in the next section.

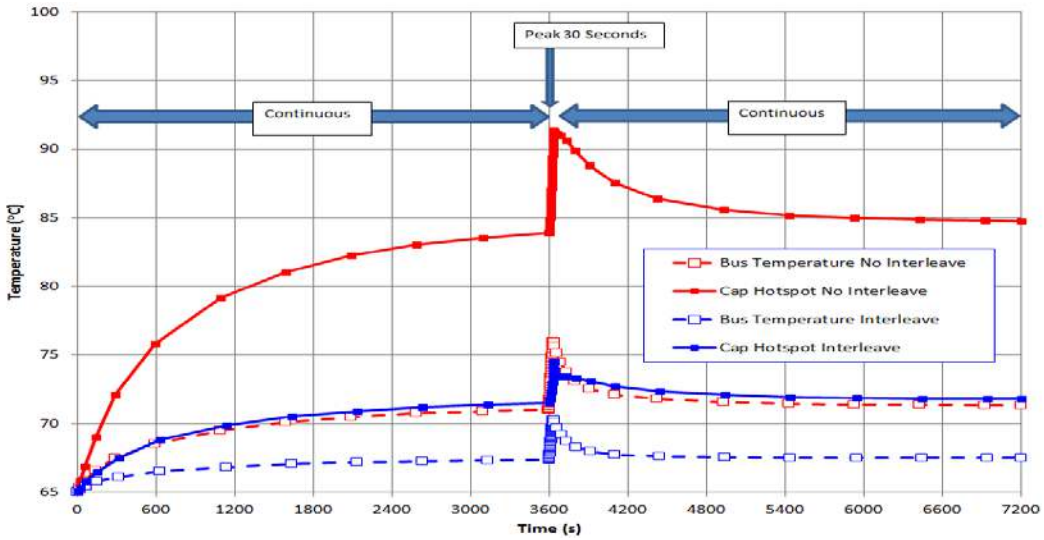

Fig. 6. Maximum capacitor winding and bus temperatures predicted for one hour of continuous operation followed by a 30 second peak operating condition at 65°C with and without interleaved PWM to reduce ripple current.

The simulation was performed assuming a 65°C cooling plate applied to the bus insulation via a high performance gap pad. The continuous operating condition was applied for one hour at which point the peak condition was applied for 30 seconds followed by another hour at the continuous condition. The maximum capacitor winding temperature versus time assuming the worst case of no interleaving in the PWM is presented in the red curve with solid square markers in Figure 6. The corresponding bus temperature is provided in the red dashed curve with empty square markers. Given a maximum short time hotspot temperature limit of 107°C for metallized polypropylene, this scenario can be supported with a coolant temperature of up to 80°C. However, hofer eds has proposed the use of interleaved PWM to reduce the overall capacitor ripple current by up to nearly 50%. Taking this approach a much more optimistic scenario can be defined. Keeping the same DC current and losses, but reducing the total capacitor ripple current by nearly 50% from 192Arms to 100Arms continuous provides a significant reduction in capacitor temperature rise as shown in the blue curve with solid square markers in Figure 6. The corresponding bus temperature is shown with the dashed blue line with hollow square markers. In this case, the cooling plate temperature could be safely increased to 95°C while still respecting the capacitor hotspot limit. Note that with interleaved PWM, the capacitor hotspot temperature rises much less relative to the bus temperature. This shows that the capacitor winding hotspot is dominated by the internal losses and thermal resistance to the bus. However, the effect of bus heating will be superimposed on the capacitor losses, so the bus heating must be acknowledged for both cases.

The scenarios presented here are quite pessimistic relative to a practical drive cycle where “continuous” is typically defined in 10s of minutes rather than hours. Having defined the thermal time constants, the temperature rise subject to actual steps in the power can be evaluated for the various portions of a drive cycle. The peak current rating of the IGBT must be similarly considered in looking at the life of the system. The question remains as to which component ultimately defines the limit. In any case, the capacitor can provide more than 10,000 hours of life operating continuously at rated voltage and 95°C hotspot. This translates into a coolant temperature of 75°C without interleaved PWM and 87°C with interleaved PWM. In reality, the true nature of the drive cycle will allow even higher

coolant temperatures given much shorter continuous operation.

6.0 Power Module Heating of the DC Link

The results presented thus far have not addressed the effect of heating the cap/bus from the power module terminals.

A second 700A243 prototype was provided to Infineon Technologies for high current DC testing to develop the dual module inverter thermal model presented in Figure 7. Note that the model is built in a Foster Network representation using the test results shown in Figure 8. The power module is in this example of the HybridPACK™ Drive directly fluid cooled.

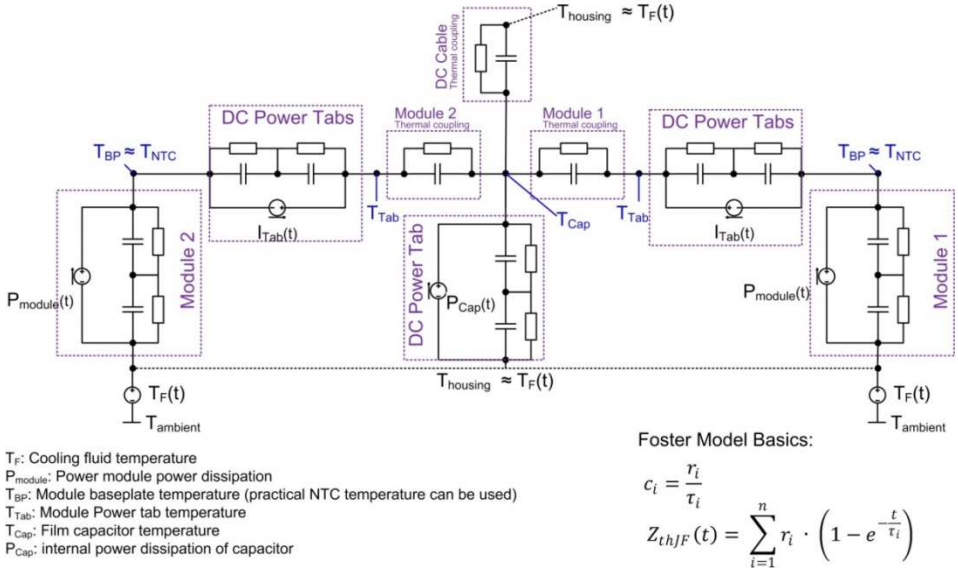

Fig. 7. Behavioral thermal model for dual power module inverter and capacitor including the power tab connection and the thermal coupling paths. For single inverter applications the half side of the model can be applied.

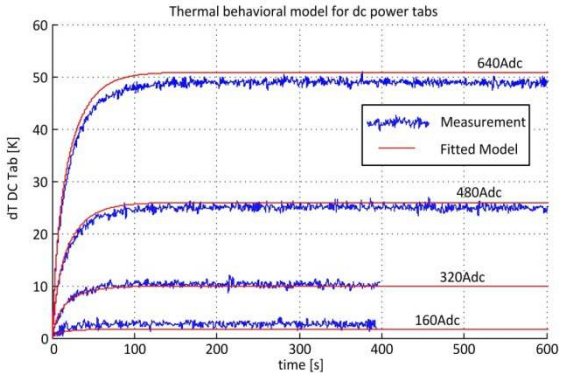

Fig. 8. Comparison of behavioral thermal model with experiments. Heating of the power module power tabs in combination with the SBE 700A243 capacitor.

The internal chip thermal behavior can be predicted quite accurately without knowing the surrounding parts. But as soon as the DC power tab connection or the capacitor heating itself has to be estimated it is hardly possible to do this without regarding the thermal coupling between module and capacitor.

When the parts are defined, the parameters of such a behavioral model can be carried out by some experiments.

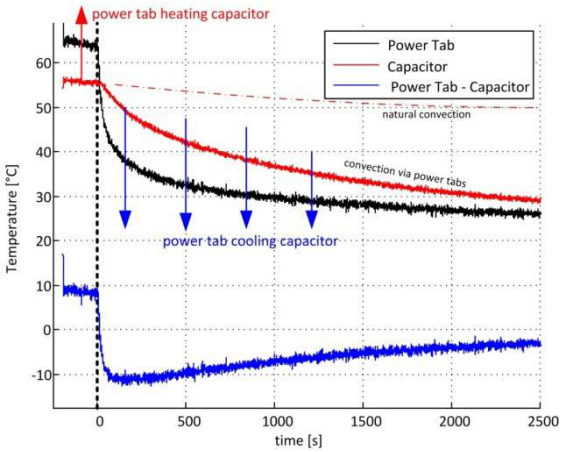

Fig. 9. Heat coupling between power tabs and the capacitor for a single module connected. The power module tabs can cool the capacitor in light load conditions especially when the capacitor was heated before due to a high vehicle acceleration event.

When the module power tabs are running hot, as in a high acceleration condition, they are heating the capacitor bus bar. But designing with the HybridPACK™ Drive will not lead to added heating for normal acceleration events. The ultrasonic welded power tabs on the module internal ceramics substrate provides an excellent thermal connection path into the cooling fluid. When power tabs are quite cool in the light load conditions they can also cool the capacitor. In order to prove this cooling, an inverter with a single power module connected was investigated in an experiment. Figure 9 shows that the capacitor was initially heated to a hot condition. The power tabs were running even hotter (about 10°C higher than the capacitor). At 0s the power module was cooled down and consequently the power tabs also cool down immediately. As soon as the power tabs are cooler than the capacitor, they extract heat and cool actively the capacitor. In this experiment the power tabs were cooled 10°C lower compared to the capacitor and within 600s the capacitor was cooled about 15°C. This 15°C heat extraction of the capacitor via the power tabs into the cooling fluid over a single module is an impressive result compared to about 2-3°C in the case of only natural convection of the capacitor. It should be noted that mounting two modules on each side of the capacitor would theoretically double this effect.

Having characterized the thermal interaction between the IGBT module power tabs and the DC link capacitor, the impact on the rating curves of Figure 6 can now be discussed. Consider the worst case capacitor hotspot temperature plot without interleaved PWM (red curve with solid red boxes):

1) 0 to 3600 seconds (continuous): The model predicts that the IGBT will actually cool the capacitor by a few degrees, thus reducing the temperature rise.
2) 3600 to 3630 seconds (peak): The IGBT power tabs will be at the same temperature as the capacitor/bus and thus no heat transfer will occur. No impact on the capacitor hotspot peak transient temperature.
3) 3630 to 7200 seconds (continuous post peak): The heat generated in the power tabs during the peak condition will very quickly be absorbed by the IGBT module coolant. Once this has occurred, the power tabs will cool the cap/bus thus reducing the temperature rise.

While these results may at first seem counter intuitive, one must recognize the improvements in the HybridPACK™ Drive module relative to conventional IGBT packages. The elimination of frame bond wire connections in favor of ultrasonic welded power tabs and improved thermal coupling to the cooling substrate clearly makes a significant difference in this case which is not representative of older generation IGBT modules. This effectively eliminates the traditional issue of heating the DC link bus due to losses in the power module DC connection tabs and bond wires. The capacitor hotspot temperatures shown in Figure 6 are thus very representative of the worst case condition.

7.0 Conclusion

The use of a single 700A243 500μF integrated and highly optimized capacitor/bus DC link to source two inverter stages using the HybridPACK™ Drive has been investigated. The results show that this concept is clearly feasible for two parallel 150kW inverters if the system level optimization is properly considered. Efficient cooling of the DC link bus bar is a requirement such that the optimal capacitor terminal structure has access to the required coolant temperature. Similarly, utilizing an advanced PWM scheme with interleaving can significantly reduce the capacitor ripple current and capacitor temperature thus allowing for hotter coolant. While the single cap/bus can work without interleaving, the capacitor hotspot temperature could exceed safe limits for long term life in the case of a very high performance system. Interleaving of the PWM provides nearly a 50% reduction in the capacitor ripple current and significantly reduces the capacitor hotspot temperature rise for a given power condition. Previously, implementation of

interleave in double inverter solutions with two separate power stages (module + DC-link) was more challenging due to possible resonance effects between the two DC-link capacitors and yielded less advantages due to distribution of the whole needed capacitance into two separate housings. The optimized internal design of the HybridPACK™ Drive module further improves the situation by eliminating additional heat loading of the DC link from IGBT losses and in fact providing some cooling of the bus.

The ability to utilize a single DC link cap/bus for two parallel inverters has significant implications in cost, size, and weight savings for dual motor inboard drive applications as well as high performance single motor (6-phase) applications especially in combination with the use of interleave. This approach cannot be realized with the conventional approach of treating the capacitor, bus, and switch modules as separate components. However, a system level approach has demonstrated that the single high performance DC link sourcing two inverter stages is quite feasible. Full scale testing with two functional inverters is planned as the next step in this development.

8.0 References

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