Low Inductance – Low Temp Rise DC Bus Capacitor Properties Enabling the Optimization of High Power Inverters

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The Power Point Presentation will be available after the conference.

Abstract

High power density converter design is a fundamental requirement to meet the challenging performance, size, reliability, efficiency, and cost goals. PEM engineers use faster IGBTs that enable designs to meet these goals. Choosing the optimal bus structure is critical and drives the need for connections to minimize inductance and achieve optimal power density. Annular capacitors provide higher current carrying capability and lower temperatures, creating the opportunity to explore new bus options.

1. Introduction

The SBE Annular form factor, Metallized Polypropylene (MPP) Film Capacitor enables low inductance (ESL) and low internal resistance (ESR) at levels previously not fielded in transportation and alternative energy inverter designs.

Extremely low ESLs can allow the inverter designer seeking optimized converter efficiency the opportunity to integrate components in a way which can eliminate component costs (i.e. snubber capacitors, balancing resistors, bus structure size and weight, and DC Link capacitance volume). As valuable as low ESL is to the optimum design, there is much confusion in the industry as to accurate ways to measure the contributing element ESL of the discrete DC Link capacitor to that of the overall desired system ESL. This paper will express SBE's method of determining low value capacitor ESLs (2 – 20nH) in a way that can be accurately be applied to switch design simulation tools for inverter optimization.

Extremely low ESRs enable very low temperature rise in the DC bus capacitor for any given ripple current requirement. The understanding and best utilization of this characteristic enable the designer to optimize efficiency of high power inverters and to understand any implications of long-term reliability. The paper will explain system design advantages to being able to accurately measure the ESR and what impact it has on temperature rise within the capacitor based on a time period and current basis. When collaboratively investigated with the inverter duty cycle waveforms of power expectations at the system level, decisions on optimization can be made with direct and defendable knowledge of the impact in terms of reliability that such desired optimization will have on the final inverter design. The reliability impacts of the decision being the result of elevated temperature inside the capacitor and ultimately the result this elevated temperature will have on dielectric reliability. The paper will then provide the reader with an example of one such customer case utilizing drive cycle power information applied to the capacitor temperature rise simulation information available at SBE. Reliability implications will be highlighted.

2. DC Link Capacitor ESL Measurement Techniques

Use of a traditional RLC bridge for measuring DC Link capacitor ESL is often of limited value for the case where the DC link capacitor has been constructed with multiple terminal pairs to reduce that ESL.

SBE has developed a test method that can be used to determine the total inductance from DC Link capacitor windings to the switch device terminals, and for some bus topologies the Capacitor ESL contribution to that inductance can also be extracted.

The test method is simple in concept, charge the DC link capacitor to a low voltage and discharge it with a short circuit located at the switch semiconductor DC supply terminals. At the instant the short circuit occurs, a damped cosine voltage is developed across the capacitor as shown in Fig. 1.

This circuit behavior will be typical of all DC link capacitor/interconnect assemblies. The loop inductance of the capacitor and interconnect can be determined by classical circuit analysis for an under-damped series RLC circuit. The capacitance can be measured, and the damped oscillation frequency can be inferred from the oscilloscope trace captured at the discharge. A very close estimate of loop inductance can be obtained from: $L = (1/C)*(1/(2\pi f))^2$.

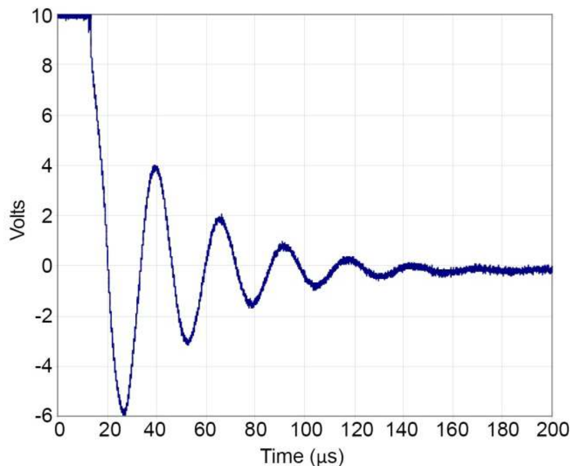

Fig. 1. DC link discharge waveform as measured with oscilloscope

The devil is in the required "bus short circuit device" attributes:

1. Minimal added inductance
2. No contact “bounce” [prior to completion of response to shorting operation]
3. Fast closure [relative to the system response]
4. VERY low contact resistance
5. Relatively long life [on the order of hundreds of closures]
6. Repeatable "on resistance" [relative to rest of the system R]

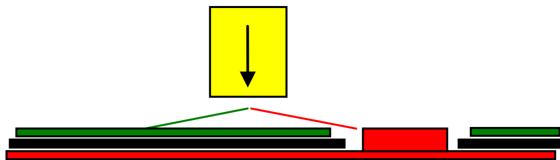

Fig. 2. Concept diagram for the DC link capacitor shorting device

Fig. 2. illustrates the best configuration obtained to date. The drawing is a cross section view of a coplanar bus. For convenience say the green layer is negative, and the red layer is positive, with the black layer the insulation. The switch is composed of the red and green outlined features. These switch contacts are constructed from ½" x ~0.040" copper strips. They are attached to the bus with brass fasteners. Not shown are the fasteners or bus relief areas needed to allow their use. However, if the bus features designed for attaching the semiconductor switch modules are used as the location for the shorting device, there should be few implementation issues. Contact between the switch strips and the bus can be enhanced by the use of conductive epoxy on the interface surfaces. The yellow rectangle represents a pneumatically driven nylon cylinder that rapidly impacts the top of the switch assembly to initiate the discharge. The switch contacts are driven together as the tips are rotated toward the bus assembly by the nylon "plunger". This arrangement eliminates the contact bounce problem, and the nylon actuates the switch fast enough for the reasonably clean "start of discharge" displayed on an oscilloscope [See Fig. 1]. The loop area under the switch contacts must be minimized as it may be a major factor in the total bus/capacitance ESL.

The extra inductance imposed by the shorting switch as described above may be less than the semiconductor switch package inductance. The relatively small cross section bond wires inside the switch package will have high inductance compared with their length. This component of the total inductance seen by the semiconductor die during turn-off is out of the ability of the product design engineer to influence but it will surely impact the turn-off voltage transient seen by the semiconductor die itself.

Semiconductor devices as "shorting switches" were not seriously considered. While there are low voltage FETs with sub milliohm on state resistances, the total loop resistance with mechanical shorting contacts can easily be sub milliohm. A sufficiently low resistance semiconductor shorting device would require many devices in parallel, would be bulky, and would add more inductance than will a mechanical switch.

Fig. 3 shows a representative power ring capacitor/coplanar bus assembly, built to provide a test vehicle and be a concept piece to illustrate the use of the DC link capacitor for a 3-phase inverter application. The left side of this bus assembly has features that show DC connection to 3 half bridge modules. The slots represent the location of the gate drive pins of the IGBT module used to create this bus assy. The right side of the bus was to illustrate an ideal location for DC input. The shorting contacts [per Fig. 2] were installed across the center switch half bridge DC input terminal locations on a bus structure similar to Fig. 3, with the capacitor and bus structure solidly mounted such that the contacts could be pneumatically closed as previously described. During the test, the bus DC input connections [on right side of bus, Fig. 3] are used to connect the charging supply and the oscilloscope [Fig. 4].

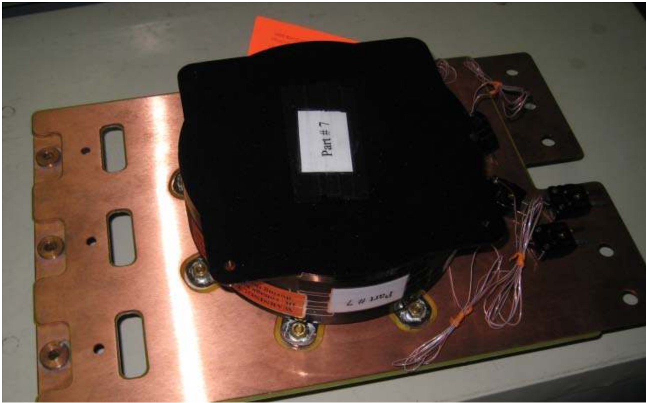

Fig. 3. SBE power ring capacitor with coplanar bus

The bus/capacitor inductance can be determined from the scope display [Fig. 1]. Calculate the time for 2 or three cycles, using the zero crossing time reference. Find the resonant frequency. The loop inductance is approximately: $L = (1/C)*(1/(2\pi f))2$.

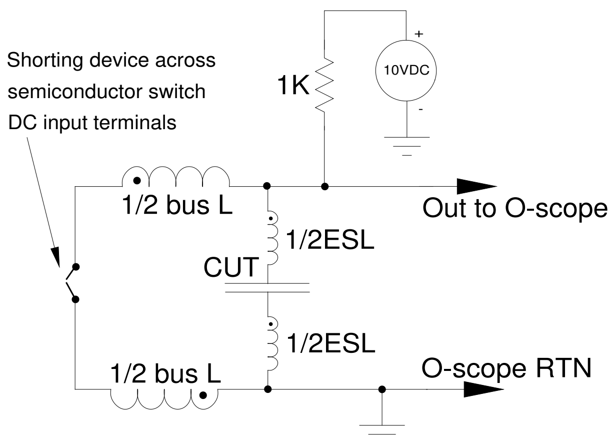

Fig. 4. Equivalent circuit of the shorting test assembly (resistance elements not shown).

This does not define capacitor ESL, only the shorted loop inductance but there is a way to determine that [for this bus topology]. If one looks at the Fig. 1 waveform, it can be seen that at the very start of the discharge there is about a 2V step before the cosine wave starts. This is the result of the voltage divider created by the capacitor ESL and the bus inductance [Fig. 4]. This voltage divider is defined by ESL/(ESL+busL).

For the case of the waveform in Fig. 1, we can say that:

2V = 10V[ESL/(ESL+busL)]

So, using the Fig. 1 waveform, we have the following:

Time for 3 complete oscillations is ~75 µsec. P = 75/3 = ~25 µsec. f = 1/P = ~40KHz

For Fig 1 waveform, assume C is 1000 µF.

Loop L = $(1/C)*(1/(2\pi f))^2$ = ~15.8nH

Now we can solve for a value for capacitor ESL:

2V = 10V[ESL/(ESL+busL)]

Capacitor ESL = ~3.2nH

... low enough to warrant interconnect optimization!

It must be noted that single minded pursuit of low inductance DC Link capacitors that connect directly to switch semiconductor modules may result in difficult to solve thermal management problems for the capacitor involved. Although the percentage of switch semiconductor losses that heat their terminals is very small, these losses transferred to the capacitor terminals can be substantially higher than the capacitor losses!

3. Performance implications of low temperature rise

Once a design has been optimized to reduce bus inductance and voltage overshoot, it is important to understand how the capacitor temperature will limit system performance. The heat generated within the annular capacitor is very small; a 700D348 1000µF capacitor carrying 200ARMS dissipates less than 6W. SBE has developed temperature profiling tools which can be iterated with design changes and external conditions. For example, Fig. 5 shows simulated and measured temperature rise for the case where a laminated bus is held at constant temperature. The reference location within the capacitor for the data in Fig. 5 was at the axial center of the winding at the radial distance where the terminals are attached to current collecting copper braid. The "noise" seen in the measured data curve is due to the resolution increments of the thermocouple data acquisition system and the cycling of the temperature chamber refrigeration system.

The same simulation tools allow detailed analysis of the temperature profile within the capacitor, [Fig. 6] and include electromagnetic and thermal effects of all capacitor components, not just the winding. This temperature contour map [Fig. 6] shows a cross section view of the capacitor through the axial center, with the axial center at the left edge of the drawing, with copper terminals and braid interconnect shown at the top and bottom of the winding.

Carefully measured materials parameters are included in these simulations. By holding the laminated bus

temperature constant, one can see how the capacitor losses raise its internal temperature above the laminated bus temperature. It is important because other thermal input to the laminated bus is likely much higher than the power ring capacitor losses.

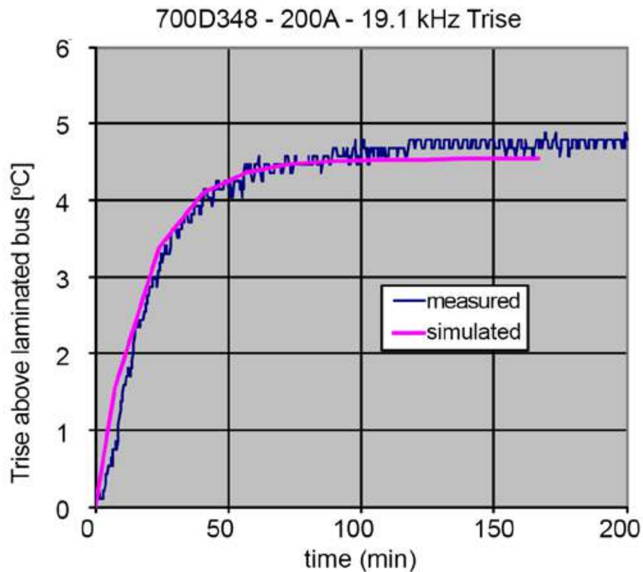

Fig. 5. Measured and simulated Trise for a 1000µF Power Ring

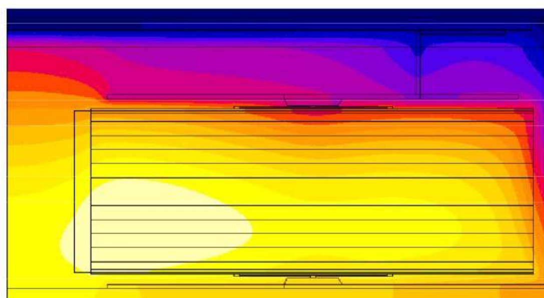

Fig. 6. 700D348 1000µF power ring temperature profile at 200ARMS, 19.1KHz

These other laminated bus heat sources are:

- AC and DC conduction losses,
- interconnect losses [especially those carrying AC], and
- thermal input from the switch semiconductor modules.

The latter can be quite significant in watts, even though this is only a very small % of the total switch semiconductor loss. The resulting Trise will affect the capacitor and ultimately the system reliability. In a real system, the capacitor will be mounted such that some heat is conducted to that mounting location. If the temperature difference between the laminated bus and the capacitor is more than a few degrees celsius, the capacitor assembly becomes a thermal path for laminated bus heat, and the capacitor winding hot spot is located where the terminals attach to the winding. Use of the capacitor as a mechanism to cool the laminated bus is not necessarily a bad thing as long as the designer is aware of the situation and temperatures do not exceed design guidelines. Minimizing the bus temperature rise is a worthy goal that will enhance inverter reliability.

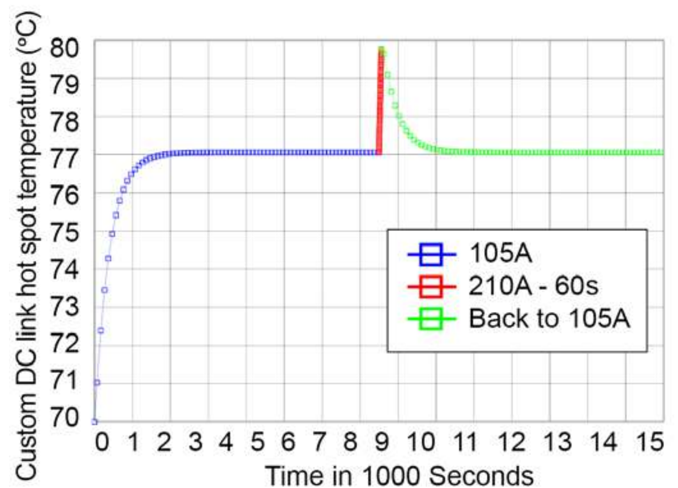

Fig. 7. Transient thermal response

For power conversion applications where full load must be continuous, the entire thermal environment must be carefully considered to ensure the capacitor remains as cool as possible for enhanced system reliability. For electric vehicle applications, full load will be unlikely for a significant time compared with the thermal time constant of the DC link capacitor. Fig. 7 shows the transient thermal response for a relatively small custom DC link capacitor. This simulation was done to examine the Trise expected if the capacitor current was doubled for one minute. This represents a 4-fold increase in capacitor dissipation, and a rapid temperature rise. The rate of rise is limited by the relatively high specific heat of polypropylene, and the result was that the hot spot Trise was less than 3°C over this period. The temperature rise for any particular electric vehicle "drive cycle" can be simulated. Since the thermal time constant is so long, the output power of the inverter could be

temperature limited if necessary to keep the capacitor temperature below some set point. Keep in mind that the above simulation was done assuming only capacitor dissipation. In a real system, the thermal input to the capacitor from the previously discussed bus losses would also be increased by a factor of 4.

4. Details on how ESR/ESL impacts inverter design plus show various options

It is important now to discuss the implications of lower Temperature Rise, lower ESL, and lower ESR on the design and performance of the inverter. Before beginning any design project with a Ring Capacitor, it is critical to identify the critical constraints on the project to ensure key goals are achieved. Inverter projects can be broken down into three general categories as follows:

A. Drop in Replacement - the design specification is complete, however, there is an opportunity to replace the traditional capacitors with Ring Capacitors by leveraging the same space;
B. Modification to an Existing Design - the volumetric size and dimensions of the design specification are complete, however, there is an opportunity to change the internal layout and connections of the active and passive components;
C. Complete New Design - the design specification has not been defined and there is an opportunity to explore new options without the constraints of an existing design.

Application of the Ring Capacitor technology into each of these three categories will yield improved performance, however, the more flexibility in the design parameters, the more opportunity exists for a breakthrough in W/cm^3, cost, reliability, and size. The ability to achieve high density design goals for inverters is directly impacted by the constraints on the development cycle.

As discussed, the unique temperature rise characteristics of the Ring Capacitor enable the development of a low inductance co-planar bus structure. The capacitors allow for short, equal length connections while delivering high current handling capability. In addition, ring capacitor connection systems allow for direct connection of the capacitor to the heat sinks thus achieving lower temperatures. Careful attention must be put on the losses transferred to the capacitor terminals as the capacitors are mounted closer to the IGBT Modules. Simulation tools are a necessary tool to understand the unintended consequences of making these changes**.**

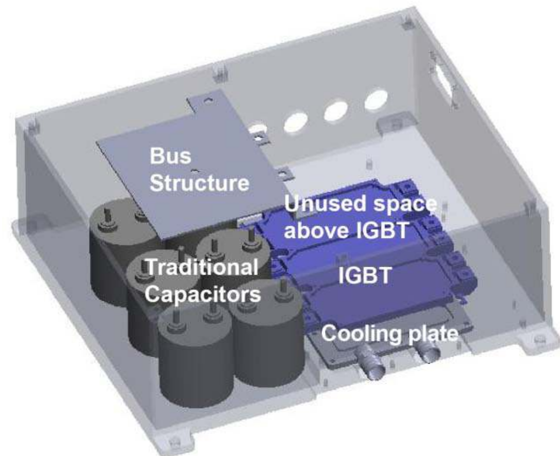

Fig. 8: Typical planer inverter layout

The net result is a tighter, more compact inverter design with significantly reduced voltage overshoot and switching losses. Several inverter designs from categories A, B, and C above have emerged using the Ring Capacitor, however, due to space constraints this paper is going to only explore a Modification to an Existing Design called the "stacked" inverter. Please contact SBE for further discussion about additional reference designs for inverters.

The "stacked" inverter design evolves from modifying a typical automotive inverter by utilizing the excess space left above the IGBT module (see figure 8). By bending the end of co-planar bus plate (see figure 9), the IBGT, die, cooling plate, and the ring capacitor are “stacked” on top of each other in a symmetrical fashion. The ring capacitor is placed underneath the cooling plate. The cooling plate is shared with the IGBT module which is mounted on the top. Figure 10 shows the “stacked’ inverter design after the integration of the ring capacitor and the co-planar bus plate. It should also be noted that in some design examples, the “stack” is inverted with the capacitor is on the top of the stack and the IGBT modules are on the bottom. The resulting advantages are the same in either configuration. It is the designer’s choice which one is on the top vs. the bottom.

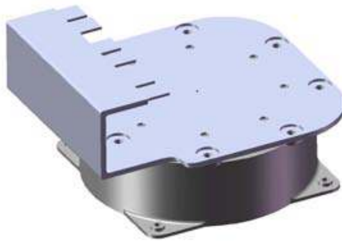

Fig. 9: Annular Capacitor with vertical enabling bus plate- “cap on bottom” implementation

Depending on the dimensions and specifications of the existing design, a "stacked" design can deliver up to 30% volume reduction and W/cm^3 based solely on the vertical integration process. With these improvements come weight reductions and cost reductions due do less film, potentially less bus materials, less packaging materials and the possible elimination of snubbers depending on choices made.

The final total inductance of the stacked vertical design has to be carefully considered when choices are being made. If care is not taken as to how long the “loop” portion of the folded over bus is, the resulting inductance could become unacceptably high.

Of course, if you look at figure 10, you will see that the width of the required cooling plate for both the capacitor and the IGBT modules is directly proportional to the length of the bend in this configuration.

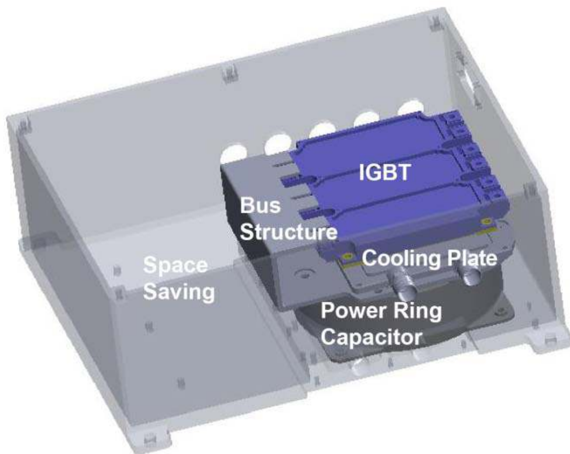

Fig. 10: Stacked Vertical IGBT – Cap arrangement

There is also the ability to integrate the low ESR characteristics of the annular shape into the final design for further reduction of volume of the capacitor itself for a given power density or to minimize cooling needs, and thereby reducing overall bus inductance. By now combining both aspects of vertical integration and the low temperature rise characteristics of the capacitors, an increase to 50% or more volume reduction is realistically possible (spatial reduction and capacitor volume size reduction). And by using the simulation tools now available and validated, such achievements can be done without sacrifice of system reliability.

5. Conclusion

This paper has shown that ESL and ESR are very important characteristics for DC Link capacitors in the inverter application. The measurement of ESL, especially at the <10nH level, is not straightforward but can be done accurately. Such information is important as it will have significant effects on IGBT switch waveform and transient characteristics and could help reduce cost (possible elimination of snubbers) and improve the quality of the output waveform when the correct, informed decisions are made by the designer.

The ESR value is important in that it directly translates into temperature rise under load in the inverter. By understanding the temperature rise of the capacitor under all drive cycle conditions, the proper cooling decision can be made to insure reliable life of the capacitor and ultimately the inverter. As such, the cooling system does not need to be oversized unnecessarily.

The paper has shown a specific example of transforming a traditionally aligned planar bus structure IGBT – DC Link capacitor structure into a vertically stacked arrangement. This arrangement can reduce volumetric space and weight by up to 50% with no sacrifice in reliability. This can be safely done by understanding the important capacitor characteristics of ESL and ESR and applying the known values to the design process and making the best decisions for low inductance and thermal management under all drive cycle loads. By applying the technical advance “dividends” to the resulting inverter design, reliability, size, weight, and cost can all be optimized.

Future work includes additional optimization designs where the application has volumetric and/or dimensional flexibility. Additional future work will be taking advantage of the thermal transfer characteristics of the bus structure itself as a way to further remove heat from the system and increase reliability for a given power density level.

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